

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1.-115. (Cancelled)

116. (Currently amended) ~~[[The]]~~ A semiconductor structure of claim 113 comprising:
a layer structure including a uniform, substantially relaxed etch-stop layer having a
doping level below 10^{18} atoms/cm³,
wherein the uniform etch-stop layer comprises a silicon dioxide layer.

117.-125. (Cancelled)

126. (Currently amended) ~~[[The]]~~ A semiconductor structure of claim 125 comprising:
a layer structure comprising a uniform etch-stop layer having a doping level below 10^{18}
atoms/cm³ and a substantially relaxed layer,
wherein the relaxed layer is graded.

127. (Previously presented) The semiconductor structure of claim 126, wherein the relaxed layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

128. (Previously presented) The semiconductor structure of claim 127, wherein $x < 0.2$.

129. (Previously presented) The semiconductor structure of claim 128, wherein the uniform etch-stop layer comprises substantially relaxed $\text{Si}_{1-y}\text{Ge}_y$ and $y > 0.19$.

130.-132. (Cancelled)

133. (Currently amended) ~~[[The]]~~ A semiconductor structure comprising: of claim 132
a layer structure including a uniform etch-stop layer having a doping level below 10^{18}
atoms/cm³,
wherein the layer structure comprises a substantially relaxed layer disposed under the
uniform etch-stop layer and a first strained layer disposed over the uniform etch-stop layer.

134. (Currently amended) The semiconductor structure of claim ~~[[132]]~~133, wherein the first strained layer comprises $\text{Si}_{1-z}\text{Ge}_z$ and $0 \leq z < 1$.

135.–139. (Cancelled)

140. (Previously presented) A semiconductor structure, comprising
a layer structure including a strained $\text{Si}_{1-z}\text{Ge}_z$ layer, and
a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer,

wherein $0 \leq z < 1$, the layer structure includes a substantially relaxed uniform etch-stop layer disposed over a substantially relaxed layer comprising graded $\text{Si}_{1-x}\text{Ge}_x$, the strained $\text{Si}_{1-z}\text{Ge}_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

141. (Currently amended) A semiconductor structure comprising:
a layer structure including a strained $\text{Si}_{1-z}\text{Ge}_z$ layer~~[[,]]~~;
a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer; and

an insulator layer disposed over the layer structure,
wherein $0 \leq z < 1$, the layer structure includes a substantially relaxed uniform etch-stop layer disposed over a substantially relaxed layer, the strained $\text{Si}_{1-z}\text{Ge}_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

142. (Currently amended) A semiconductor structure comprising:
a layer structure including a strained $\text{Si}_{1-z}\text{Ge}_z$ layer~~[[,]]~~; and
a handle wafer comprising an insulator, the layer structure being bonded to the handle wafer~~,
[[; and]]~~

wherein $0 \leq z < 1$, the layer structure comprises a substantially relaxed uniform etch-stop layer and substantially relaxed graded layer disposed over the substantially relaxed layer, the

strained $\text{Si}_{1-z}\text{Ge}_z$ layer is disposed over the uniform etch-stop layer, and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

143. (Previously presented) The semiconductor structure of claim 142, wherein the substantially relaxed graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

144.–158. (Cancelled)

159. (Previously presented) A semiconductor structure comprising:

- a first uniform etch-stop layer;
 - a second etch-stop layer disposed over the uniform etch-stop layer;
 - a substantially relaxed layer disposed over the second etch-stop layer;
 - a substrate disposed over the relaxed layer; and
 - an insulator layer disposed over the ~~strained~~ substantially relaxed layer, between the relaxed layer and the substrate,
- wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

160. (Previously presented) A semiconductor structure comprising:

- a first uniform etch-stop layer;
 - a second etch-stop layer disposed over the uniform etch-stop layer;
 - a substantially relaxed layer disposed over the second etch-stop layer; and
 - a substantially relaxed graded layer,
- wherein the first uniform etch-stop layer is disposed over the graded layer and the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

161. (Previously presented) The semiconductor structure of claim 160, wherein the substantially relaxed graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

162. (Previously presented) The semiconductor structure of claim 160, further comprising:

a first substrate,

wherein the substantially relaxed graded layer is disposed on the first substrate.

163. (Previously presented) A method for forming a semiconductor structure, the method comprising:

forming a uniform etch-stop layer;

providing a handle wafer; and

bonding the uniform etch-stop layer directly to the handle wafer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

164. (Previously presented) The method of claim 163, wherein the uniform etch-stop layer comprises substantially relaxed Si_{1-y}Ge_y.

165. (Previously presented) The method of claim 163, further comprising:

planarizing a surface of the uniform etch-stop layer prior to bonding.

166. (Currently amended) A method for forming a semiconductor structure, the method comprising:

forming a uniform etch-stop layer;

providing a handle wafer;

bonding the uniform etch-stop layer to the handle wafer; and

forming a substantially relaxed graded layer before forming the uniform etch-stop layer,

wherein the uniform etch-stop layer is formed over the substantially relaxed graded layer and said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

167. (Previously presented) The method of claim 166, wherein the relaxed graded layer comprises Si_{1-x}Ge_x.

168. (Previously presented) The method of claim 166, further comprising:

releasing the etch-stop layer by removing at least a portion of the graded layer.

169. (Previously presented) The method of claim 166, wherein releasing the etch-stop layer comprises a wet etch.

170. (Previously presented) The method of claim 166, further comprising:
providing a semiconductor substrate,
wherein the substantially relaxed graded layer is formed over the semiconductor substrate.

171.-176. (Cancelled)

177. (Currently amended) A method for forming a semiconductor substrate, the method comprising:

providing a first substrate;
forming a layer structure over the first substrate by:
forming a uniform etch-stop layer over the first substrate; and
forming a strained layer over the uniform etch-stop layer; and
releasing the strained layer by removing at least a portion of the uniform etch-stop layer,
wherein the uniform etch-stop layer has a relative etch rate which is less than
approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

178. (Previously presented) The method of claim 177, wherein releasing the strained layer comprises a wet etch.

179. (Currently amended) A[[The]] method of claim 171 for forming a semiconductor structure, the method comprising:

providing a first substrate; and
forming a layer structure over the first substrate by:
~~wherein forming the layer structure comprises~~ forming a substantially relaxed graded layer over the first substrate, and
forming a [[the]] uniform etch-stop layer is formed over the graded layer, the uniform etch-stop layer having a doping level below 10^{18} atoms/cm³.

180. (Previously presented) The method of claim 179, wherein the graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

181. (Previously presented) A method comprising:

providing a first substrate;

forming a layer structure over the first substrate by:

forming a substantially relaxed graded layer over the first substrate;

forming a uniform etch-stop layer over the graded layer;

forming a strained layer over the uniform etch-stop layer; and

releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer,

wherein the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

182. (Previously presented) The method of claim 181, wherein releasing the strained layer comprises a wet etch.

183.–187. (Cancelled)

188. (Previously presented) A method for forming a semiconductor structure, the method comprising:

forming a layer structure by:

forming a uniform etch-stop layer; and

forming a strained $\text{Si}_{1-z}\text{Ge}_z$ layer over the uniform etch-stop layer, and

bonding the layer structure to a handle wafer comprising an insulator; and

releasing the strained layer by removing at least a portion of the uniform etch-stop layer,

wherein $0 \leq z < 1$ and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

189. (Previously presented) The method of claim 188, wherein releasing the strained layer comprises a wet etch.

190. (Previously presented) A method for forming a semiconductor structure, the method comprising:
forming a layer structure by:
 forming a substantially relaxed graded layer;
 forming a uniform etch-stop layer over the substantially graded layer; and
 forming a strained $\text{Si}_{1-z}\text{Ge}_z$ layer over the uniform etch-stop layer, and
bonding the layer structure to a handle wafer comprising an insulator,
wherein $0 \leq z < 1$ and the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.
191. (Previously presented) The method of claim 190, wherein the relaxed graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.
192. (Previously presented) The method of claim 190, further comprising:
 releasing the strained layer by removing at least a portion of the graded layer and at least a portion of the uniform etch-stop layer.
193. (Previously presented) The method of claim 192, wherein releasing the strained layer comprises a wet etch.
194. (Previously presented) The method of claim 190, further comprising:
 forming an insulator layer over the layer structure.
195. (Previously presented) The method of claim 190, further comprising:
 providing a substrate,
 wherein the layer structure is formed over the substrate.
196. (Previously presented) The method of claim 195, further comprising:
 releasing the strained layer by removing at least a portion of the substrate, at least a portion of the graded layer, and at least a portion of the uniform etch-stop layer.

197. (Previously presented) The method of claim 196, wherein releasing the strained layer comprises a wet etch.

198.–199. (Cancelled)

200. (Currently amended) A[[The]] method of claim 199, for forming a semiconductor structure, the method comprising:

forming a strained etch-stop layer; and

forming a substantially relaxed $\text{Si}_{1-w}\text{Ge}_w$ layer over the etch-stop layer,

wherein $w > 0$, the etch-stop layer comprises $\text{Si}_{1-z}\text{Ge}_z$ and $z = 0$.

201.–203. (Cancelled)

204. (Currently amended) A[[The]] method of claim 203 for forming a semiconductor structure, the method comprising:

forming a first uniform etch-stop layer;

forming a second etch-stop layer over the uniform etch-stop layer; and

forming a substantially relaxed layer over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³, the second etch-stop layer comprises strained $\text{Si}_{1-z}\text{Ge}_z$, and $z = 0$.

205.–207. (Cancelled)

208. (Currently amended) A[[The]] method for forming a semiconductor structure, the method of claim 206, further comprising:

forming a first uniform etch-stop layer;

forming a second etch-stop layer over the uniform etch-stop layer;

forming a substantially relaxed layer over the second etch-stop layer;

bonding the substantially relaxed layer to a substrate comprising an insulator; and

releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

209. (Previously presented) The method of claim 208, wherein releasing the second etch-stop layer comprises a wet etch.

210. (Previously presented) The method of claim 208, further comprising:
releasing the substantially relaxed layer by removing at least a portion of the second etch-stop layer.

211. (Previously presented) The method of claim 208, wherein releasing the substantially relaxed layer comprises a wet etch.

212. (Currently amended) ~~A[[The]] method of claim 201, further~~ for forming a semiconductor structure, the method comprising:

forming a first uniform etch-stop layer;

forming a second etch-stop layer over the uniform etch-stop layer; and

forming a substantially relaxed layer over the second etch-stop layer,

forming a substantially relaxed graded layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³, and the first uniform etch-stop layer is formed on the graded layer.

213. (Previously presented) The method of claim 212, wherein the substantially relaxed graded layer comprises Si_{1-x}Ge_x.

214. (Previously presented) The method of claim 212, further comprising:
bonding the substantially relaxed layer to a substrate comprising an insulator.

215. (Previously presented) The method of claim 212, further comprising:

releasing the first etch-stop layer by removing at least a portion of the relaxed graded layer.

216. (Previously presented) The method of claim 215,
wherein releasing the first etch-stop layer comprises a wet etch.

217. (Previously presented) The method of claim 215, further comprising:
releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

218. (Previously presented) The method of claim 215, wherein releasing the second etch-stop layer comprises a wet etch.

219. (Previously presented) The method of claim 217, further comprising:
releasing the relaxed layer by removing at least a portion of the second etch-stop layer.

220. (Previously presented) The method of claim 219, wherein releasing the relaxed layer comprises a wet etch.

221. (Currently amended) A[[The]] method of claim 201, further for forming a semiconductor structure, the method comprising:

providing a first substrate; and

forming a layer structure over the first substrate by:

forming a substantially relaxed graded layer over the first substrate[[;]],

forming a first uniform etch-stop layer over the graded layer,

forming a second etch-stop layer over the uniform etch-stop layer, and

forming a substantially relaxed layer over the second etch-stop layer,

wherein the first uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³, the first uniform etch-stop layer is formed over the graded layer, and the layer structure comprises the substantially relaxed graded layer, the first uniform etch-stop layer, the second etch-stop layer, and the substantially relaxed layer.

222. (Previously presented) The method of claim 221, wherein the substantially relaxed graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

223. (Previously presented) The method of claim 221, wherein the first uniform etch-stop layer comprises substantially relaxed $\text{Si}_{1-y}\text{Ge}_y$, the second etch-stop layer comprises strained $\text{Si}_{1-z}\text{Ge}_z$, $0 \leq z < 1$, and the substantially relaxed layer comprises $\text{Si}_{1-w}\text{Ge}_w$.

224. (Previously presented) The method of claim 221, further comprising:
bonding the layer structure to a second substrate including an insulator.

225. (Previously presented) The method of claim 224, wherein the second substrate comprises a material selected from the group consisting of silicon, glass, quartz, and silicon dioxide.

226. (Previously presented) The method of claim 221, the method further comprising:
releasing the first etch-stop layer by removing at least a portion of the first substrate and at least a portion of the graded layer; and
releasing the second etch-stop layer by removing at least a portion of the first etch-stop layer.

227. (Previously presented) The method of claim 226, further comprising:
bonding the layer structure to a second substrate prior to releasing the first etch-stop layer.

228. (Previously presented) The method of claim 226, further comprising:
releasing at least a portion of the relaxed layer by removing at least a portion of the second etch-stop layer.

229. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a first substrate;

forming a layer structure on the first substrate by:

forming a substantially relaxed graded layer on the first substrate; and

forming a uniform etch-stop layer on the graded layer; and

releasing the etch-stop layer by removing at least a portion of the substrate and at least a portion of the graded layer,

wherein the uniform etch-stop layer of $\text{Si}_{1-y}\text{Ge}_y$ has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

230. (Previously presented) The method of claim 229, wherein the substantially relaxed graded layer comprises $\text{Si}_{1-x}\text{Ge}_x$.

231. (Previously presented) The method of claim 229, wherein the uniform etch-stop layer comprises substantially relaxed $\text{Si}_{1-y}\text{Ge}_y$.

232. (Previously presented) The method of claim 229, further comprising:
bonding the layer structure to a second substrate prior to releasing the etch-stop layer.

233. (Cancelled)

234. (Currently amended) ~~A[[The]] semiconductor structure of claim 112 comprising:~~
a layer structure including a uniform etch-stop layer having a doping level below 10^{18}
atoms/cm³.

wherein the etch-stop layer comprises n-type dopants.

235. (Currently amended) ~~A[[The]] semiconductor structure of claim 112 comprising:~~
a layer structure including a uniform etch-stop layer,
wherein the etch-stop layer comprises p-type dopants and the doping level is below 4×10^{16} atoms/cm³.

236.-238. (Cancelled)

239. (Previously presented) A method for forming a semiconductor structure, the method comprising:

forming a layer structure including a uniform etch-stop layer;

providing a handle wafer; and

bonding the layer structure directly to a handle wafer,

wherein said uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of Si doped with 7×10^{19} boron atoms/cm³.

240.-241. (Cancelled)